DIGITAL LOGIC

COURSE CODE: BCA 103

YEAR/SEMESTER: I/I **CREDIT HOURS: 3**

WORKLOAD: 6 HOURS A WEEK LECTURE: 3 Hrs. **PRACTICAL: 3 Hrs.**

Course description

This course familiarizes students with fundamental concept of digital logic system, Number System, principles and properties of Boolean algebra and its application in simplification, gate implementation, Understand and Design Functions of Combinational Logic, Sequential Logic, Programmable Logic Devices. It also covers the use of flip flops in the design of synchronous and asynchronous sequential logic circuits.

Course objectives

- To provide the concepts used in the design and analysis of digital systems
- To enable student to design combinational logic circuit
- To enable student to design sequential logic circuit and programmable memory.

Course contents

1	**Digital Design Fundamentals and Number System**	**8 hrs**
1.1	Analog and digital Signal	
1.2	Analog and digital System	
1.3	Number System Representation	
1.4	Number System and their Conversion	
1.4.1	Binary Number System	
1.4.2	Octal Number System	
1.4.3	Decimal Number System	
1.4.4	Hexadecimal Number System	
1.5	Representation of signed numbers, Floating point number	
1.6	Complement of Number Systems	
1.6.1	r's complement	
1.6.2	r-1's complement (with r as 2 or 10)	
1.7	Binary Arithmetic	
1.8	Representation of BCD, ASCII, Excess 3, Gray Code, Error Detection Codes	

2 Boolean Algebra and its simplification **8 hrs**

2.1 Basic Logic Gates: AND, OR and NOT

2.2 Universal Logic Gates: NAND and NOR

2.3 Extended/Derived Logic Gates: Ex-OR and Ex-NOR

2.4 Boolean Algebra

2.4.1 Postulates and Theorems

2.4.2 Canonical Forms(SOP, POS)

2.4.3 Simplification of Boolean Functions using laws

2.5 Simplification of Logic Function using Karnaugh Map

2.5.1 Analysis of SOP and POS expressions

2.6 Simplification of up to 5 variable Boolean expression using Quine-McCluskey Minimization Technique (Tabular Method)

3 Combinational Logic Design **10 hrs**

3.1 Implementation of Combinational Logic Function

3.1.1 Half Adder and Full Adder

3.1.2 Half Subtractor and Full Subtractor

3.1.3. Encoders and Decoders

3.2 Implementation of data processing circuits

3.2.1 Multiplexers and Demultiplexers

3.2.2 Parallel Binary adder

3.2.3 Magnitude comparator (2bit and 4 bit)

3.2.4 Code Converters

3.2.5 Parity Generator and checker

3.3 Basic Concepts of Programmable Logic

3.3.1 ROM

3.3.2 PAL

3.3.3 PLA

4 Sequential Logic Design **10 hrs**

4.1 Concept of Sate and State Diagram

4.2 State Reduction technique

4.3. Triggering and its types

4.4 Latches and Flip-Flops (RS,D,T,JK, Master-Slave)

5 **Counters and Registers** **12 hrs**

5.1 Asynchronous and Synchronous Counter

5.1.1 Ripple counter

5.1.2 Ring counter

5.1.3 Modulus 10 Counter

5.1.4 Modulus counter (5,7,11)

5.1.5 Synchronous Design of above counters

5.2 Registers

5.2.1 Serial in Parallel out register

5.2.2 Serial in Serial out register

5.2.3 Parallel in Parallel out register

5.2.3 Parallel in Serial out register

5.2.4 Bidirectional Shift Register

Laboratory Works [48 hrs]

Tools: Digital Logic Trainer Kit, Bread Board and Simulator

1. Familiarization with Logic Gates
2. De-Morgan's Law and its familiarization with NAND and NOR gates
3. Realization of Half Adder and full Adder
4. Realization of Half subtractor and full subtractor
5. Encoder, Decoder, Multiplexer and Demultiplexer
6. Implementation of RS and D flip flop
7. Implementation of T and JK flip flop
8. Implementation of synchronous and asynchronous counter

Required readings:

Floyd, T. L. (2011). *Digital Fundamentals.* Pearson

Mano, M. (2018). *Digital Design.* Pearson

Tocci, R.J. (2001). *Digital Systems-Principles & Application.* Pearson